ABSTRACT OF THE DISCLOSURE

The collectors of transistors are connected via respective resistances to a power supply terminal receiving a power supply voltage. The emitters of the transistors are connected to a ground terminal via respective resistances. A shunt resistance, a FET, and a shunt resistance are connected in series between nodes connected to the respective emitters of the transistors. The gate of the FET is connected via a resistance to a control terminal receiving a control voltage. The shunt resistances and FET form a variable resistance circuit.